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09/446,507	12/27/1999	KAZUO KATO	500.38017X00	2422

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EXAMINER

BOCURE, TESFALDET

ART UNIT	PAPER NUMBER
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2631

DATE MAILED: 11/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

09/446,507

Applicant(s)

KATO ET AL.

Examiner

Teskaldet Bocure

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 08 September 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☐ Claim(s) 1-17, 24, 26 and 32-38 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 24 and 32-38 is/are allowed.
- 6) ☒ Claim(s) 1, 4, 5 and 9-17 is/are rejected.
- 7) ☐ Claim(s) 2, 3, 6-8 and 26 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
- a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

1. Claims 1,4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kardontchik et al.** (US patent number 5,566,204, of a record) in view of .

**Yeh et al.** (US patent number 5,180,214, newly cited).

2. Claims 1,4 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by **Kardontchik et al.** (US patent number 5,566,204).

**Kardontchik et al.** (**Kardontchik** hereinafter) teaches a fast acquisition clock recovering circuit (fig.1) comprising: a first clock recovering circuit having a first control

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section (see phase detector) for detecting the phase difference of the received clock (see clock output from the XOR) and that of the internally generated clock (see second input from the oscillator 24); and a second control section (see frequency detector) for detecting the frequency difference of the received clock (see clock output from the XOR) and that of the internally generated clock (see second input from the oscillator 24); an oscillator for receiving the output clock control signal from the phase and frequency detector as in claims 4,5; and feedback loop controlling both the phase detector 54 and frequency detector 70 as in claim 1.

What **Kardontchik** fails to teach is that the first and second feedback loops are integral and proportional controller respectively. **Yeh et al.** for the same endeavor as the instant application and that of Kardontchik teaches a phase locking loop circuit (see figures 4,6 and 14) for controlling the phase and frequency of the internally generated clock signal comprising an integral control and proportional control for controlling the phase and frequency of the internally generated clock signal respectively.

Therefore, it would have been obvious to one of an ordinary skill in the art to use the proportional and integral controlling of **Yeh** to control the phase and frequency of the internal clock signal at the time the invention was made.

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claim 14 is rejected under 35 U.S.C. 102(e) as being anticipated by **Barrett, Jr. et al.** (US patent number 5,422,911, of a record).

**Barrett, Jr. et al.** (**Barrett** hereinafter) teaches a phase looking loop (claimed processor) comprising: means for processing the received reference clock source (claimed data) according to an externally controlled clock signal. Wherein the frequency of the phase lock loop is controlled by an external source (see frequency control bus in figure fig. 4 and 105 in figures 2 and 3) as in claim 14.

Further, **Barrett** also teaches that the transmission system in figure 1 as having an external power supply (101). However he fails to teach that the information processing apparatus of figure 1 renders a variable frequency based on the remaining charge of the battery so that the processing apparatus operates on the frequency commensurate which [with sic.] remaining charge of the battery. However it is well known in the communication system that the processor, which processes the received data, should be able to perform the function when the battery level of the power supply (101) is not in full charge. Otherwise, it is not true that the transmission system should perform all the operation only if the system's power supply is at full charge. Therefore, it would have been obvious to one of an ordinary skill in the art the system of Barrett to perform all the reception and synchronization process when the power level of the battery is less (claimed remaining charge) at the time the invention was made.

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 9,10,11,12,and 15-17 rejected under 35 U.S.C. 103(a) as being unpatentable over **Barrett, Jr. et al.** (US patent number 5,422,911, of a record) in view of **Kardontchik et al.** (US patent number 5,566,204, of a record).

**Barrett, Jr. et al.** (**Barrett** hereinafter) teaches a phase looking loop (claimed processor) comprising: means for processing the received reference clock source (claimed data) according to the controlled clock signal. Wherein the frequency of the phase lock loop is controlled by an external source (see frequency control bus and 105) as in claims 9,10,11,12 and 14.

What **Barrett** fails to teach is that the phase locking circuit as having the claimed first and second feedback circuits as in claims 11 and 16 and first and second control circuits as in claims 9,10,12 and 15.

**Barrett** also teaches that the system having an external power supply (101) as in claim 17.

**Kardontchik** for the same endeavor, phase locking loop, as the instant application and that of **Barrett** teaches a fast acquisition clock recovering circuit (fig.1) comprising: a first clock recovering circuit having a first control section (see phase detector) for detecting the phase difference of the received clock (see clock output from

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the XOR) and that of the internally generated clock (see second input from the oscillator 24); and a second control section (see frequency detector) for detecting the frequency difference of the received clock (see clock output from the XOR) and that of the internally generated clock (see second input from the oscillator 24) ; an oscillator for receiving the output clock control signal from the phase and frequency detector; and feedback loop controlling both the phase detector 54 and frequency detector 70.

Therefore it would have been obvious to one of an ordinary skill in the art to use the frequency difference circuit detector for correcting the frequency at the time the invention was made.

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Ooishi** (US patent number 5,783,956, newly cited) in view of **Kardontchik et al.** (US patent number 5,566,204, of a record).

**Ooishi** teaches a clock distribution system (fig.1) for distributing a synchronized clock signal to a plurality of circuits within the system comprising: a phase lock loop having a phase and frequency detector for generating an phase and frequency control signal (see col. 5, lines 8-123) to control the oscillator (6); and an external power supply for supplying power to the system (see for example the abstract) as in claim 13.

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What **Ooishi** fails to teach is the claimed first and second feedback loops for controlling the phase and frequency of the oscillator. **Kardontchik** for the same endeavor as the instant application and that of **Ooishi** teaches a phase locking loop having a first and second loops (see input to the phase detector and frequency detector in figure 1) for controlling the phase and frequency of the oscillator as is the case in the system of **Oaishi**. Therefore, it would have been obvious to one of an ordinary skill in the art to use a separate feedback loops of **Kardontchik** in the system of **Oaishi** in order to control separately the phase and frequency errors of the oscillator at the time the invention was made.

#### ***Allowable Subject Matter***

9. Claims 24 and 32-38 are allowed.
10. Claims 2,3,6,7,8 and 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

#### ***Conclusion***

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US patent numbers 5,036,294 and 5,475,718 issued to Rosenkranz and McCaslin respectively disclose a phase locking loop having both proportional and integral controlling loop for controlling the phase and frequency of the oscillator.



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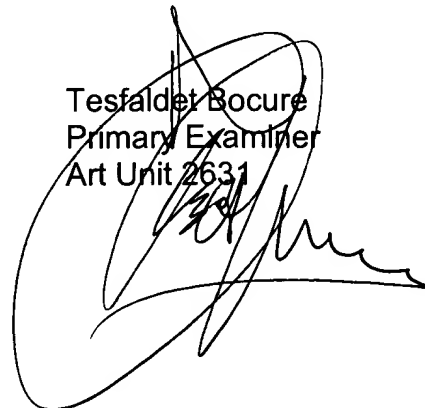
US patent numbers 5,999,039; 6,229,861 and 6,163,186 issued to Holst et al., Young and Kurita respectively disclose a phase locking loop having means for distributing clock to a plurality of circuitry with the system.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tesfaldet Bocure whose telephone number is (703) 305-4735. The examiner can normally be reached on Mon-Thur (7:30a-5:00p) & Mon.-Fri (7:30a-5:00p).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H Ghayour can be reached on (703) 306-3034. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9314.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4700.

Tesfaldet Bocure  
Primary Examiner  
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A handwritten signature in black ink, appearing to be 'T. Bocure', is written over the printed name and title of the examiner.

T.Bocure